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FLEXIBLE DCP INTERFACE

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RESEARCH FOR EFFICIENT WATER USE

Kansas State University Manhattan

FLEXIBLE DCP INTERFACE[1]

by

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ABSTRACT

A user of an ERTS data collection system (DCS) must supply the sensors and signal-conditioning interface. The electronic interface must be compatible with the NASA-furnished data collection platform (DCP). We describe here a "universal" signal-conditioning system for use with a wide range of environmental sensors.

The interface is environmentally and electronically compatible with the DCP and has operated satisfactorily for a complete winter wheat growing season in Kansas.

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INTRODUCTION

The Data Collection Platform (DCP) is a field-deployable, automatic, data-relay terminal that can be located in remote areas to gather information for specific applications or to complement imagery information received from the ERTS system. The DCP (which consists of an electronic unit, an antenna assembly, and an interconnecting cable) accepts sensor input data. The accepted data can be in the format of eight analog inputs; eight 8-bit, serial-digital inputs; eight, 8-bit, parallel-digital inputs; or combinations of these formats. To gather these data, the user must supply a power source, sensors and signal-condition system for his specific requirements[3/].

The data collection platform interface (DCPI), described here, is a "universal" signal-conditioning system that accepts inputs from 8 sensors of almost any type and interfaces them to the DCP. The DCPI contains power supplies, control logic, memory, and signal-conditioning modules for each sensor. An alteration in a signal-conditioning function can be easily affected by inserting the proper module in the DCPI. Modules can perform a variety of signal conditioning functions such as amplifying, linearizing, integrating, totaling counts, sample-hold, and comparing previous readings. Appendix A lists the sensors and signal-conditioning system used in our wheat study.

TECHNICAL DESCRIPTION

Figure 1 is a functional block diagram of the DCPI. Two 12-volt car batteries power both the DCP and DCPI. Time between recharging the battery

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[3/] Earth Resources Technology Satellite Data Collection Platform Field Installation, Operation and Maintenance Manual. NASA. Goddard Space Flight Center.

is dependent on the particular function modules; for our study, it was about 2 months under average conditions.

The 24-hour clock sends time data (in 10 minute increments) to the modules. The main controller sequentially interrogates the signal-conditioning modules and controls the data storage cycle. The analog to digital converter converts analog to digital data for storage in the memory.

The 64-bit memory stores the data from the 8 sensors (8 bits for each sensor). Data are transferred to the DCP for transmission, or back to the modules for comparison to current data.

Light emitting diodes on the instrument panel monitor the data and provide information during routine field inspections. The DCP transmits at 3-minute intervals 24 hours a day. The TRANSMIT CLOCK from the DCP shifts 64 data bits (8 per sensor) from the memory to the transmitter. After the transmission, the DCPI scans the eight channels and stores any new data in the memory. The logic flow in a scan cycle is best illustrated by specific example, like maximum-minimum temperature.

Example Logic Flow. At the start of a scan, the main controller turns on the power supply and, after a 5-second delay, interrogates channel 1. Following interrogation, logic control shifts from the main controller to the interrogated module, which then connects itself (via a set of CMOS switches) to the 10 control-buss lines. Assume that the sensor is a temperature sensor and the module is designed to find the maximum air temperature during the day. The maximum temperature module converts the resistance of the temperature sensor to a properly scaled, analog voltage, and then generates a start of conversion (SOC) command, causing the analog-to-digital converter (ADC) to convert the analog voltage from the module (ADO) line to digital data. After the digital conversion, the ADC generates an END-OF-CONVERSION (EOC) signal informing the module that the conversion process is complete.

Previous maximum temperature is stored both in an 8-bit, parallel output shift register on the module and also in the main memory. These digital data are converted (at the module) to analog and compared with current temperature. Two cases present themselves: (1) the present temperature is higher than the maximum or (2) the present temperature is lower than the maximum.

Case 1. The module sets the DATA, REPLACE-SAVE (D, R-S) line to REPLACE and generates a START-OF-STORE (SOST) command. The main controller accepts the command and generates an 8-pulse, shift-clock train (SHFT CLK). The SHFT CLK shifts the digital data from the ADC to the input of the memory and shifts the memory 8 places, thus transferring the new data into memory. The DIGITAL DATA in (DDI) line transfers the new temperature reading from the ADC to the module using the SHFT CLK signal for synchronization.

Case 2. The module sets the D, R-S line to SAVE and generates an SOST command. The main controller again generates SHFT CLK. The replace-save switch at the memory input is now set at SAVE and the memory cycles the stored data, leaving them unchanged in memory.

At the end of the storage cycle the main controller generates an END-OF-STORE (EOST) command, which resets a latch on the maximum temperature, and then interrogates Channel 2. The same type of control chain now occurs with module 2. This sequence continues until all 8 channels have been scanned.

Digital data also can be gated from the module to the main memory. Module 2, hours of free moisture, would set the DATA, ANALOG-DIGITAL (D,A-D) line to digital. Digital data gated by SHFT CLK proceeds from the module on the DIGITAL-DATA-OUT (DDO) line, through the analog-digital switch, directly to the memory. The replace-save function is operable in the digital as well as the analog data mode.

The sequence of INT, SOC, EOC, SOST, and EOST is repeated for each module. After the last module is interrogated, the interface turns off everything except the continuous power.

Control Cards A1 and A2 (Figs. 2 and 3).

The DCPI control section includes two circuit cards, A1 and A2. A1 contains the 64-bit memory and most of the control logic. A2 contains the analog-to-digital converter and display drivers.

At the start of a DCP transmission the DATA GATE drops low and remains for its 80 ms warmup-transmit cycle. Q1, Q2, and Q5 interface between the 5-volt DCP TTL logic and the 12-volt DCPI CMOS logic. U10D turns on V_x, a 5-volt supply for Q5 (needed during transmit only).

If a manual scan is not in progress, the LOW at the output of U9D is gated through U13B to the mode control on the 64-bit memory (U12). U12 is now in the recirculate mode and, when clocked, its data bits will leave $\tilde{Q}$, through U17 to the DCP.

At the end of the transmission U18 latches turning on a 5-volt supply (V_5) and the main $\pm$ 15-volt supply (V_S). After a 5-second warmup, counter U26 is reset and advanced to channel 1, sending a HIGH interrogate signal to module 1. Module 1 returns its analog data (if any) to the analog-to-digital converter on control card A2. Module 1 next returns a high SOC command to the ADC. The network of U3, U4, and U5 provides a delay, after the analog signal reaches the LH0042 buffer amplifier, before the A to D conversion can start. This network also assures that SOC commands from two consecutive modules will be "see" as two HIGHS, not one long continuous HIGH.

Upon completing the A to D conversion, the ADC returns an EOC pulse to the module. When ready, the module sets the D, A-D line to 1 if it is to send digital data for storage. It sets the D, S-R (DATA, SAVE-REPLACE) to 0 or 1 depending if the new data (either from the ADC or digital data from the module) are to be retained. Next, the module returns a START OF STORE (SOST) command. The 8-pulse, shift gene ator (U19, U15, U20) sends 8-clock pulses to the memory (U12); the modules; and on card A2 to U1, the ADC to serial shift register, and to U5, the memory-to display shift register. U24 gates the digital data from the ADC shift register or the module to the memory. When the storage cycle is complete, an END OF STORE (EOST) signal is sent back to the module and U26 is advanced to interrogate the next module. After the last module has been interrogated, U14B resets latch U18A, turning off the power supplies and ending the scanning cycle.

The scanning cycle can be run under manual control to observe data and control states at each important step, thus facilitating trouble shooting.

Pressing the MANUAL SCAN START button sets latch U18B, which blocks out interferring signals from the DCP transmitter and SOST signals from the modules. U18A latches on and U26 advances to interrogate module 1. Panel LED's now display the output of the analog to digital converter, whether the data in memory will be saved or replaced, and whether analog or digital data from the module will be stored. Pressing the STEP button starts the store cycle. The LED'S now display the memory contents for channel 1: either the new channel 1 data, or the previous channel 1 data which have been retained. Pressing the STEP button again advances U26 to channel 2.

Switching the DCAN, MEMORY CYCLE switch to the MEMORY CYCLE position locks the memory in the recirculate mode, thus allowing a review of the memory contents unaltered by a scan cycle.

TIME CLOCK (Fig. 4).

A crystal-controlled clock sends 24-hour time information to each module. This enables the modules to operate on time dependent data.

Crystal-controlled oscillator U1 runs at 27.96 KHz. U4 and U8 divide this frequency down to 1 pulse per 10 minutes. U3, U6, and U10 give time outputs in 10-minute increments through 24 hours. The time outputs are bussed in parallel to all the modules.

U7 gives a 14:00 signal to the four radiation modules to avoid adding identical decoding circuitry to the four modules.

MODULES

RADIATION MODULES (Fig. 5).

The radiation module is designed for silicon photocells. U1 is a current-to-voltage converter. R1 sets the gain. U2 is a buffer for the 100-second, RC network R7, C2.

A time signal to Pin 9 causes the 14:00 data to be retained in memory for the evening transmission. From 00:00 to 13:59 the DCP transmits instantaneous data.

MAXIMUM-MINIMUM-INSTANTANEOUS TEMPERATURE (Fig. 6).

This module is divided into two circuit cards and supplies data to two channels. The module outputs instantaneous temperature on one channel. The other channel is the maximum temperature between 11:30 and 23:59, or the minimum temperature between 00:00 and 11:30. Unless a front passes through, the true maximum and minimum temperatures are transmitted.

U8 and U9 form a linear thermistor thermometer using a YSI (Yellow

Spring Instruments) thermalinear network. When Pin 19 is interrogated, instantaneous temperature is sent to the controller, which converts the instantaneous analog signal to digital data. The digital data are passed back on 10 parallel lines to the input of 10-bit latch.

The returning EOC signal strobes U26, latching SAVE-REPLACE LATCH U6A and U6B if a new maximum or minimum is present. This enters the new maximum or minimum in U3. The DAC converts this to analog data. When the next channel is scanned, U4B passes the maximum or minimum to the controller.

RELATIVE HUMIDITY AND SOIL MOISTURE (Fig. 7).

This module transmits relative humidity from 00:00 to 13:59 and soil moisture from 14:00 to 23:59.

U1 is a 1200-Hz oscillator. U1C gives a high pulse during the last ¼ of the 300-Hz swuare wave at the output of U2B. U3's output is a ± 1 volt square wave which drives the RH and SM sensors through DC blocking tantalum capacitor pairs. U4 and U5 convert current through the sensor to voltage.

The output of U4 and U5 is a square wave with a high spike on the front. The spike width is proportional to the lead wire capacitance and is an error term.

U6 and U7 are precision full-wave rectifiers. U8 C and D and U9 form a sample-hold circuit that eliminates all but the last ¼ of the wave form. This technique gets rid of the lead-wire capacitance error. U8A and -B gate the RH or SM data to the next stages, depending on time of day.

LOG AMP is a logarithmic amplifier, which straightens the RH and SM curves. U10 and U11 add offset and gain to put the signal in the final form.

The relative humidity sensor works over a 2,000 ohm to 2 megohm range.

Soil moisture is read over a 200-ohm to 20,000-ohm range.

HOURS FREE MOISTURE (Fig. 8).

The presence of dew or rain is sensed by the lowered resistance of a bifilar grid. U1 drives a 27 Hz square-wave through the sensor and R1, R2. CR1, C2, and R4 rectify and filter the output. Operational amplifier U2 compares this signal with a fraction of the logic supply.

If the sensor is wet, a 36.621 ms/cycle signal from the time clock is gated into 21-stage ripple counter U3 and U4. The last 8 bits of the counter total 256 bits at 5 minutes per bit. Hours of free moisture are obtained by substracting successive transmissions.

POWERS SUPPLIES (Fig. 9).

Two 12-volt storage batteries are the main power source. The DCP requires 24 volts and the DCPI 12 volts (Fig. 9).

Continuous 12-volt power runs all the CMOS logic in the DCPI. A 12 volt to $\pm$ 15 volt converter supplies continuous operational amplifier power if needed (Fig. 9). During a transmission, a 5-volt supply turns on to interface the CMOS to TTL. During a scan, a high power 12-volt to $\pm$ 15-volt converter supplies power to the operational amplifiers, while a high power 5-volt supply powers the ADC and some TTL logic in the DCPI.

APPENDIX A

DCP SENSOR AND SIGNAL CONDITIONING CHARACTERISTICS

CH 1. Relative humidity and soil moisture

Position: in the canopy

Sensor: Type, Relative Humidity PCRC-11 sulfonated polystyrene (Phys-Chemical Research Corp.)

Span: 0-100% RH $\pm$ RH

Accuracy: $\pm$ 1% RH

Position: 30-cm depth

Sensor: Type, soil moisture block, CEL-WFD (Beckman Instruments)

Accuracy: 2% of reading

Signal Conditioning: Type, Lead-wire, capacitance-eliminating, AC ohmmeter with log amplifier for linearization.

CH 2. Hours of free moisture (dew and rain)

Position: above canopy

Sensor: Type, Bifilar array on printed-circuit board (G-10 epoxy base)

Signal Conditioning: Type, level-detecting, AC ohmmeter
Accuracy, $\pm$ 20 MS per change of sensor state with no additional cumulative error.

CH 3. Maximum and minimum temperature

Position: at top of canopy

Sensor: Type, YSI series 700 thermalinear thermistor probe. (Yellow Springs Instruments)

Signal Conditioning: Type, digital storage of max (min) and analog comparison with present temperature.

Accuracy; $\pm$ 0.25°C.

CH 4. Instantaneous temperature

Position: at top of canopy

Sensor type and accuracy: same as channel 3.

Signal conditioning: Type, thermalinear thermistor bridge

Accuracy; $\pm$ 0.15°C.

CH 5. Incoming visible radiation

Position: approximately 2m above soil surface

Sensor: Type, silicon photocell SBC 255

Instrument: (1) cosine corrected head

(2) 6 mm heat adsorbing glass (KG-3)

(3) diffusing plastic

(4) wratten 26 filter

Response: 590 to 720 nm

Construction: Built by E. T. Laboratory

Signal Conditioning: Type, Signal averaging filter

Accuracy; $\pm$ 0.3%

Response time; 10 to 90% - 220 seconds

CH 6. Reflected visible

Same as Ch 1 except sensor is faced downward

CH 7. Incoming near-infrared radiation

Position: 1.5 m above soil surface

Sensor: Type, Silicon photocell

Instrument: (1) cosine corrected head

(2) diffusing plastic

(3) wratten 88A

Construction: Built by E. T. Laboratory

Response: 730 to 1000 nm

CH 8. Reflected near infrared

Same as Ch 3 except sensor faced downward.

APPENDIX B

Parts List for Control Boards A1 and A2

U2 - Noninverting buffer, RCA CD4050AE
(schematic shows this as an inverting buffer)

U12 - 64-bit shift register, RCA CD4031AE

U17, U18, U20 - dual flip-flop, RCA CD4013AE

U19 - counter, RCA CD4022AE

U26 - counter, RCA CD4017AE
R1, R4 - 180K and R2, R40 - 120K

R3, R11, R12, R14, R17, R19, R27, R28, R35, R37, R38 - 100K

R5, R6 - 390K

R7, R8, R9 - 82K

R10 - 39K

R13 - 12K

R16, R18, R26, R29, R34, R39 - 1.2K

R21 - 470K

R23 - 1K

R24 - 68K

R25, R30, R31 - 270K

R32 - 560K

R33 - 220K

R41, R42 - 1.5M

C1, C6, C7, C8, C10, C11, C12 - .01μF

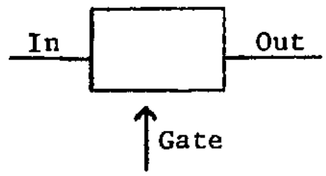
C2, C3 - 10 μF

C4, C5 - 470 pF

C9 - .002 μF

Note: (1) All digital logic parts are RCA COSMOS except where noted differently on schematics

(2) COMOS CD4016AE transmission gates are shown as



(3) NPN transistors are 2N222A

PNP transistors are 2N2907A

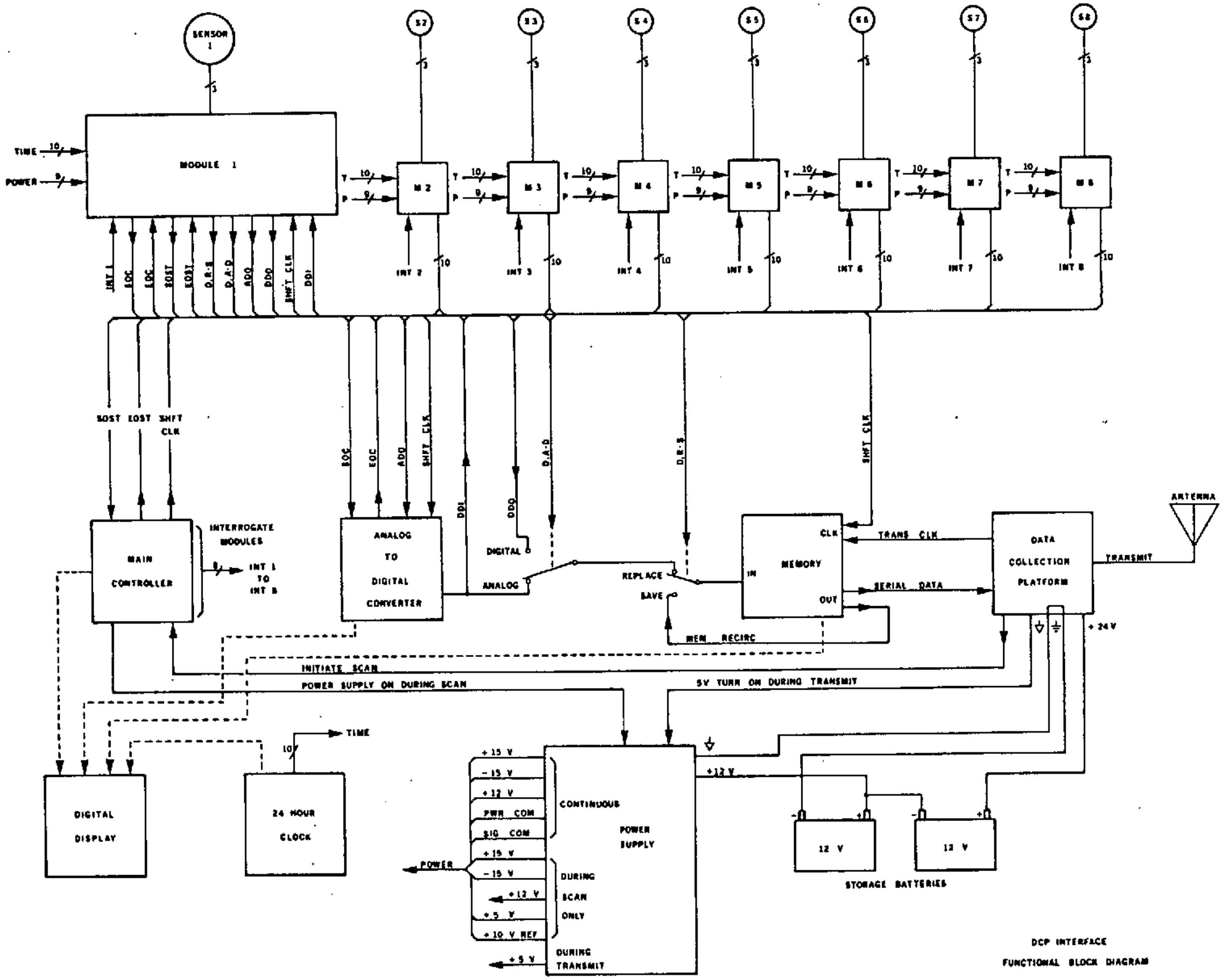


Fig. 1. DCP Interface Functional Block Diagram

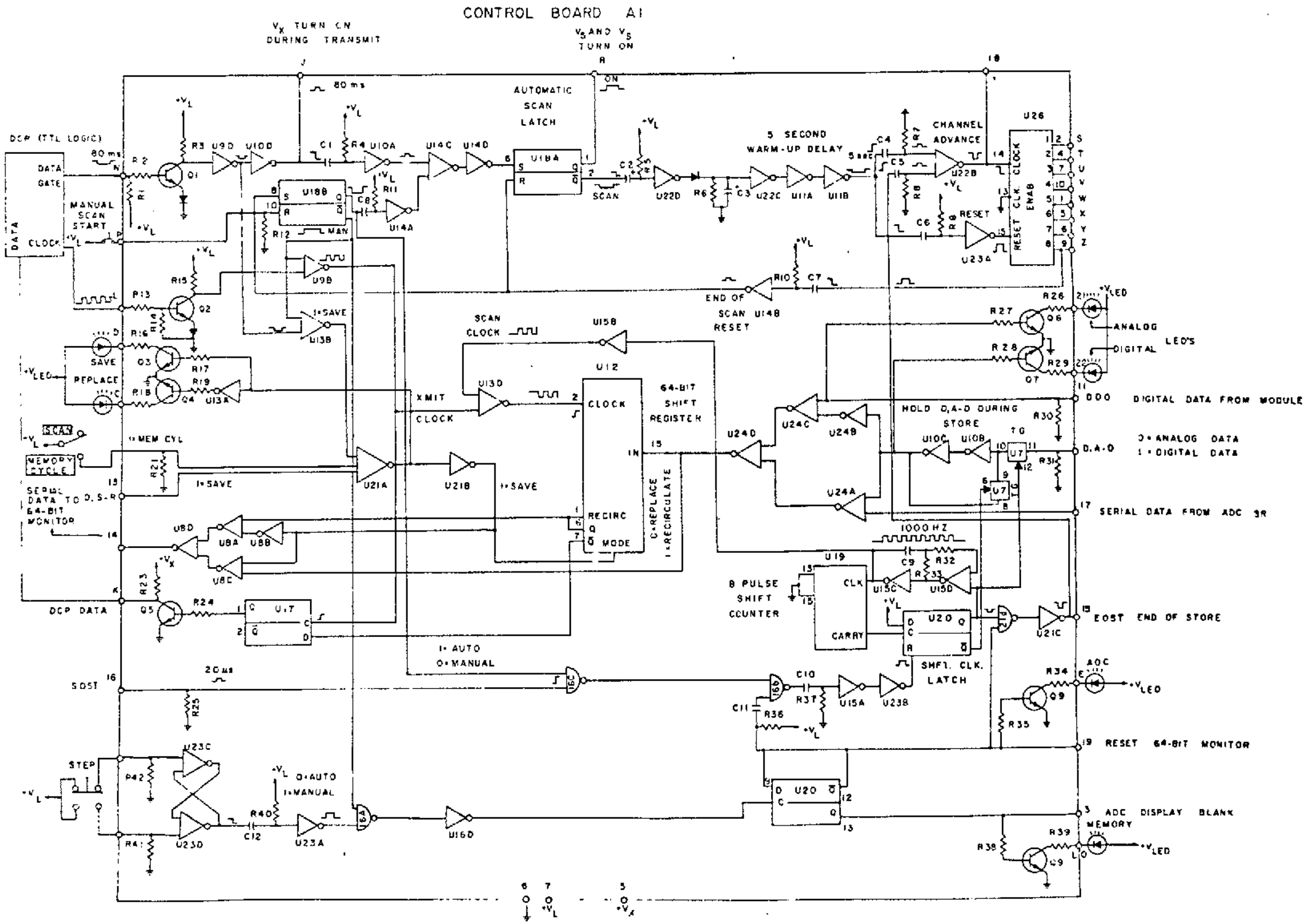


Fig. 2. Control Board A1

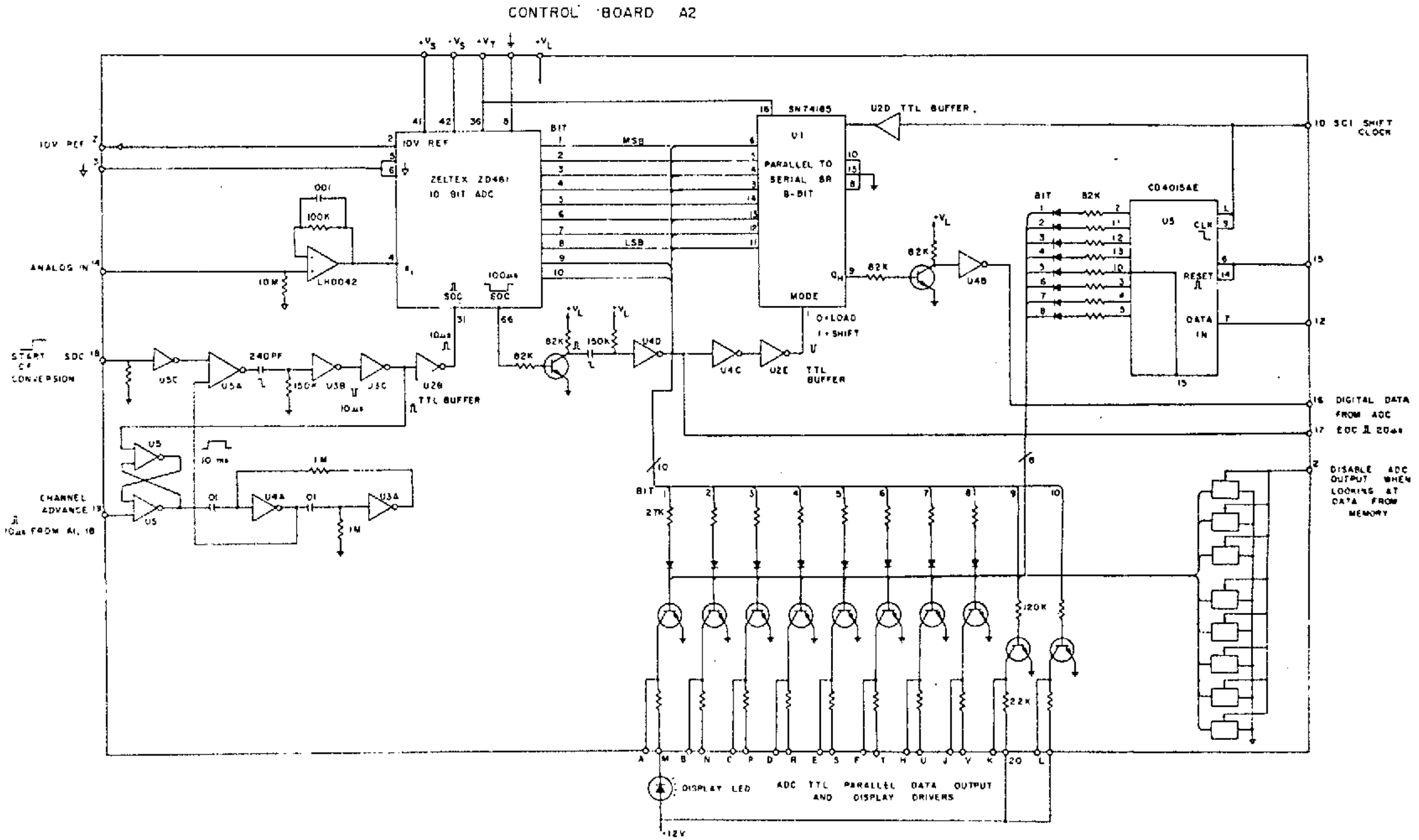


Fig. 3. Control board A2

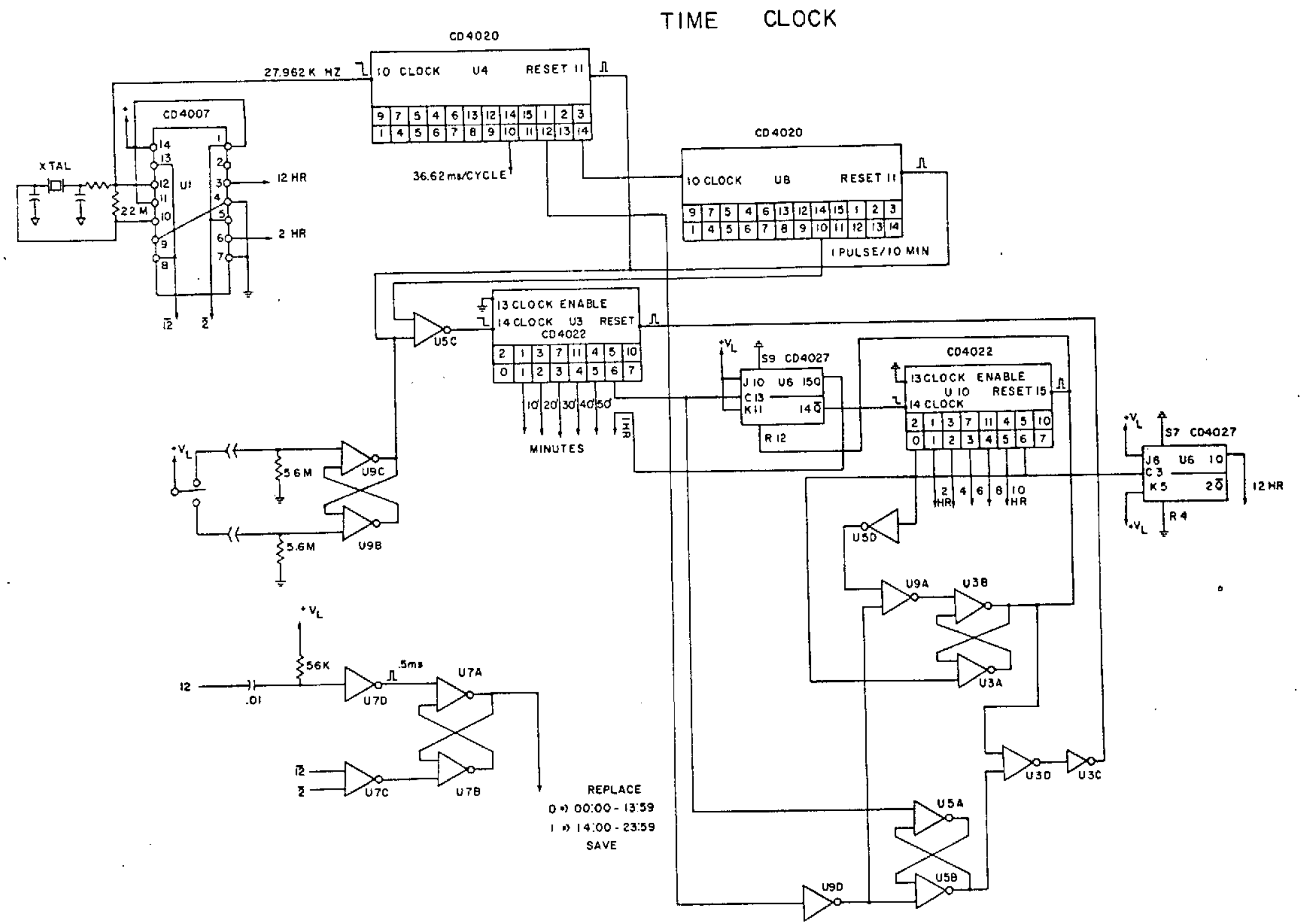


Fig. 4. Time Clock

RADIATION MODULES

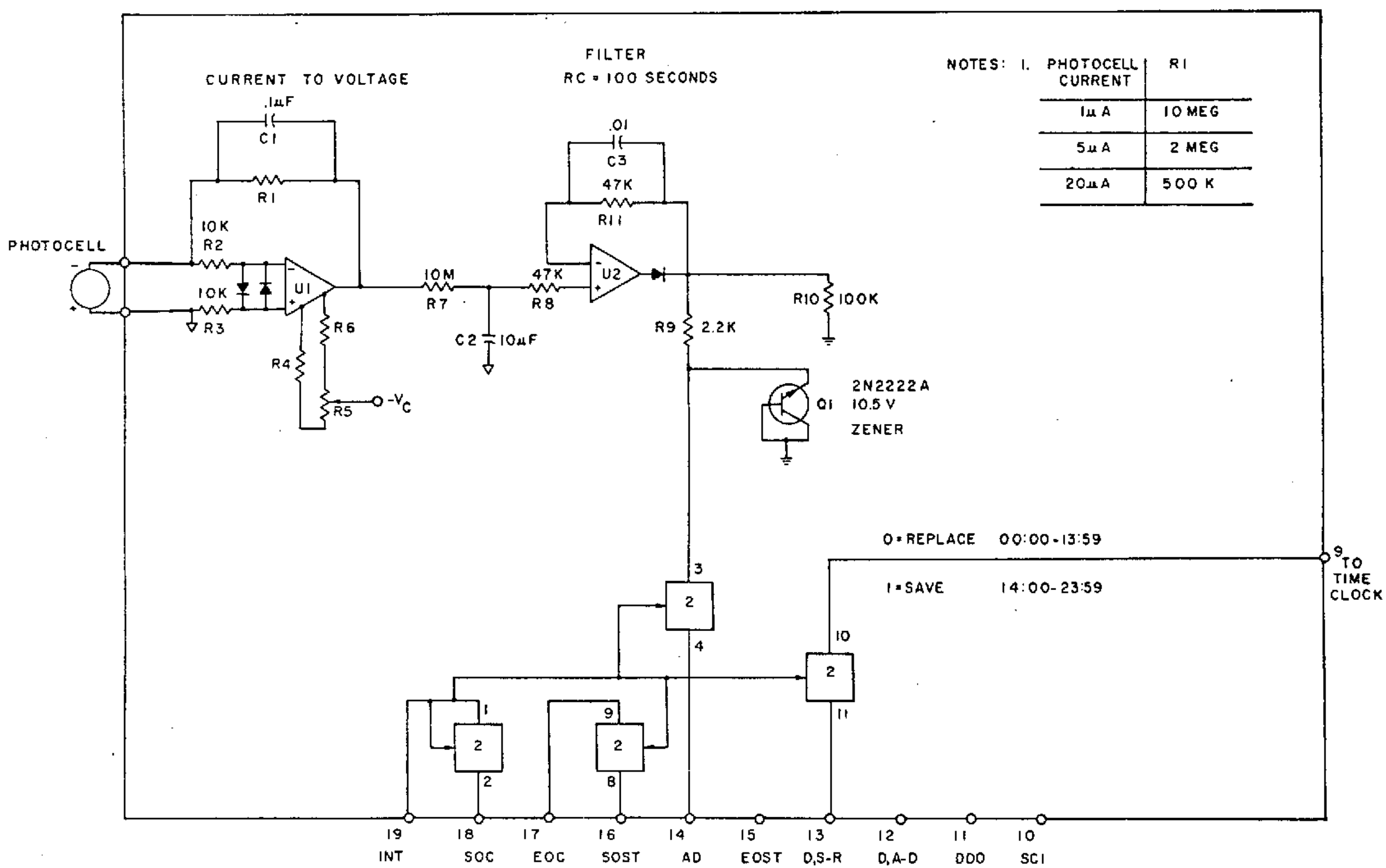


Fig. 5. Radiation Modules

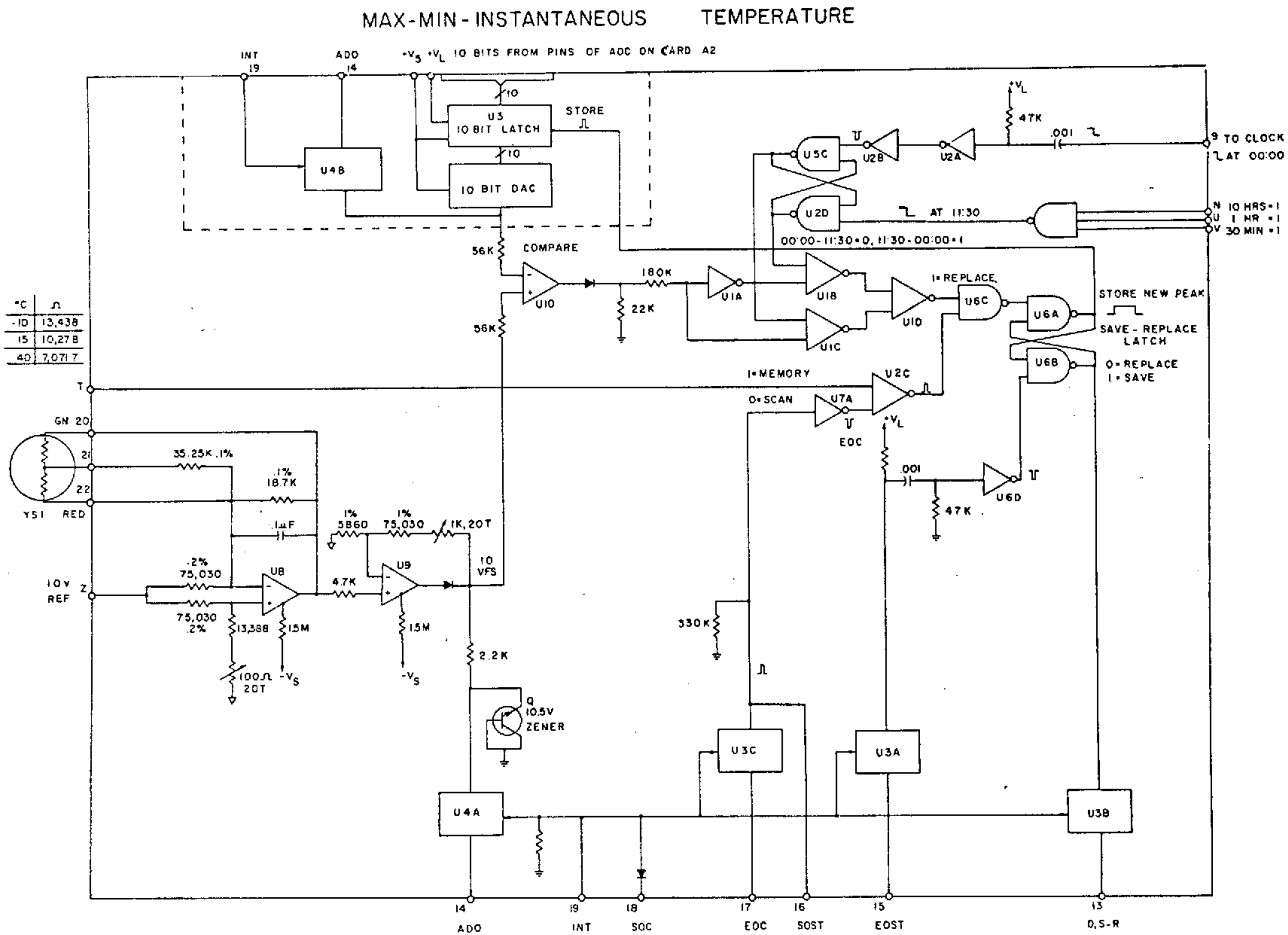


Fig. 6. Max-Min-Instantaneous Temperature

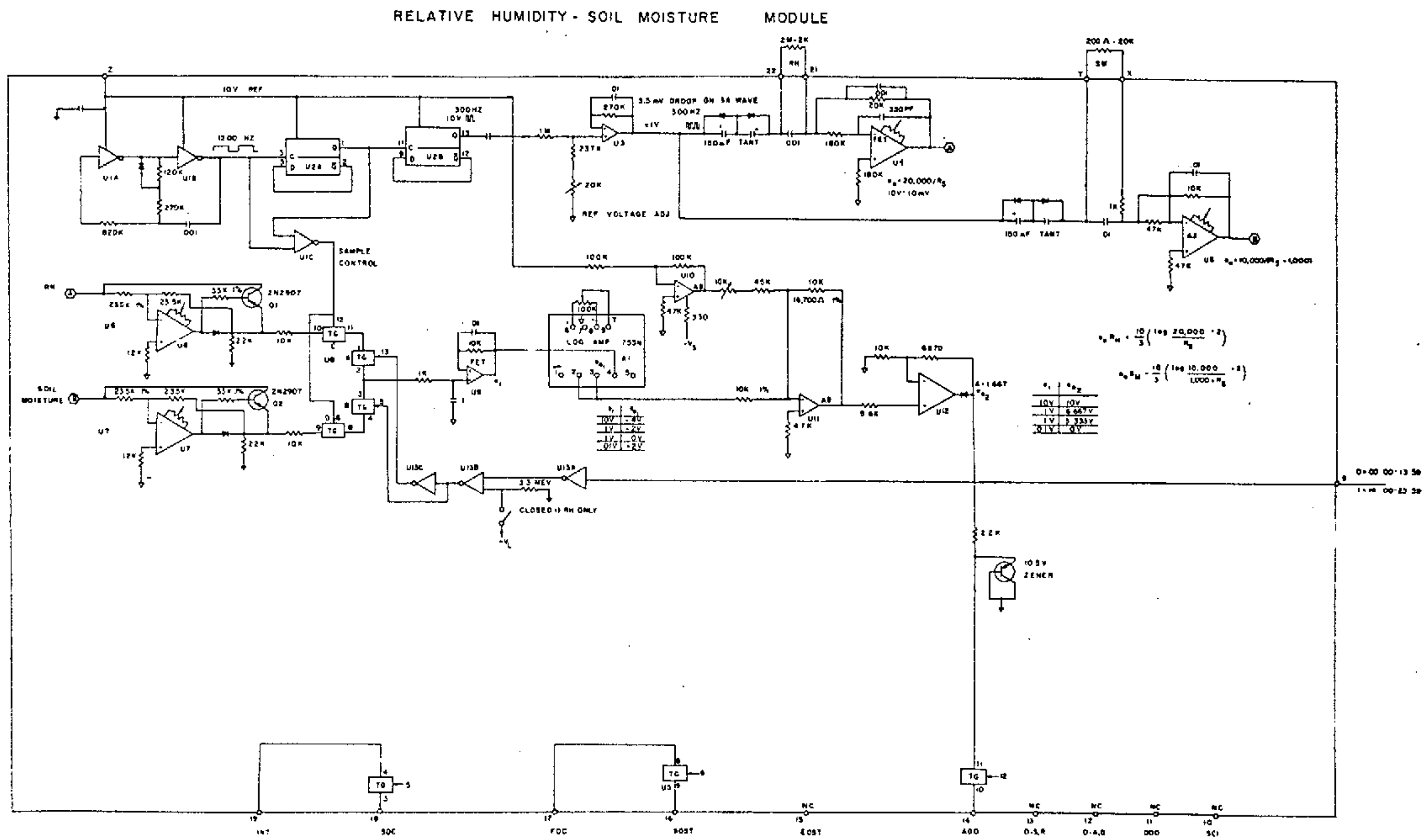


Fig. 7. Relative Humidity-Soil Moisture Module

HOURS FREE MOISTURE

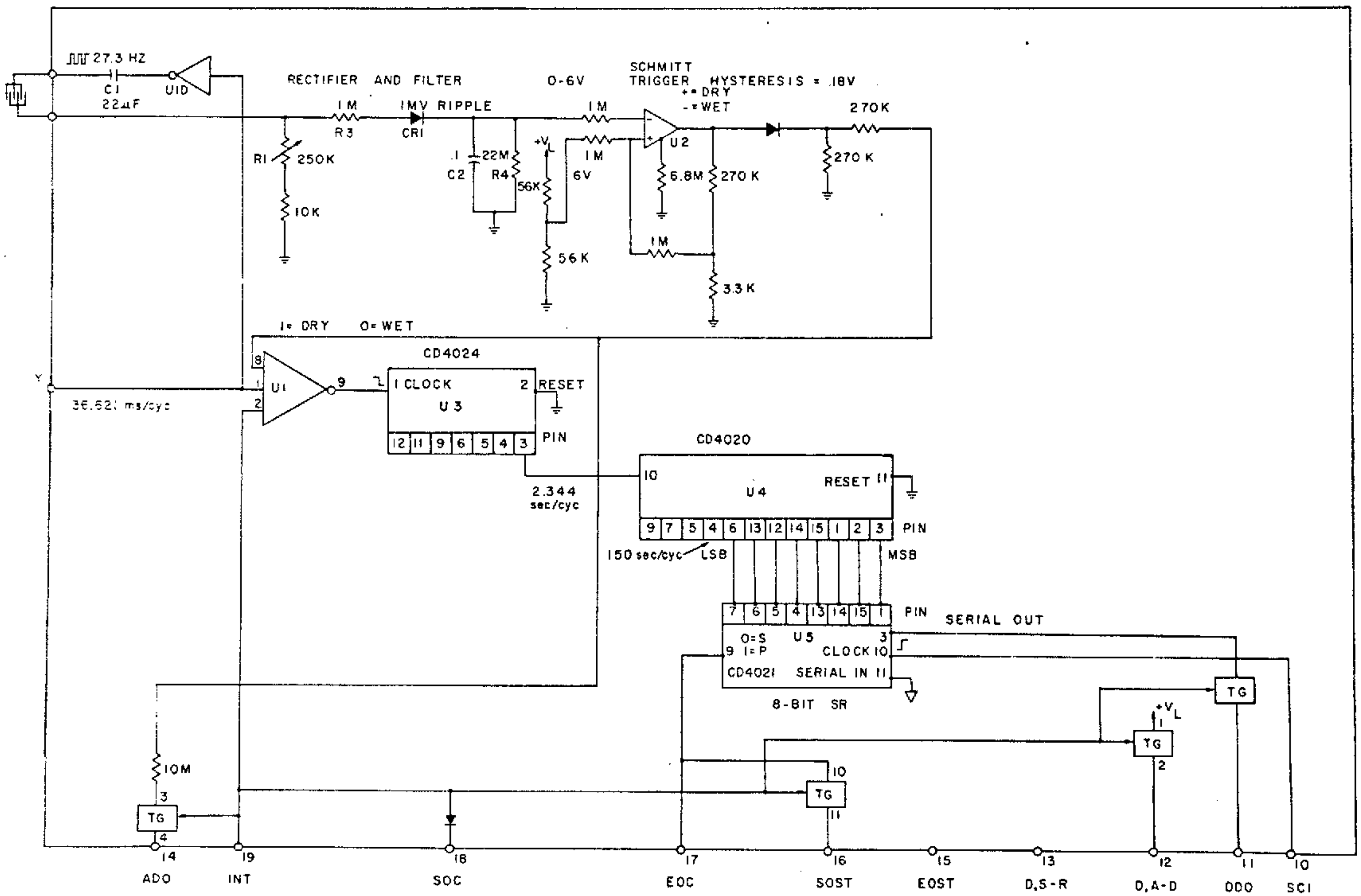


Fig. 8. Hours free moisture

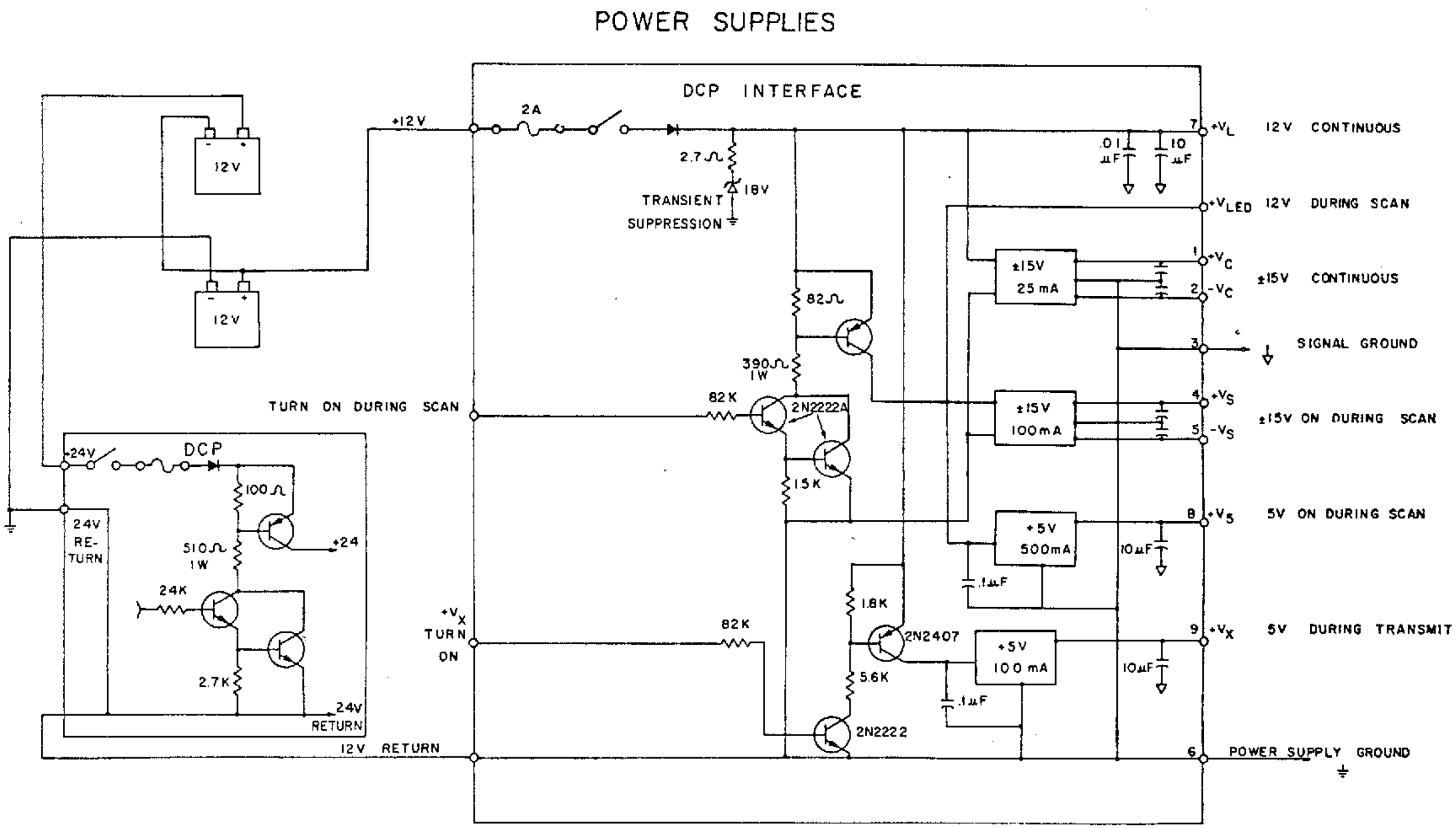


Fig. 9. Power Supplies